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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,652	07/21/2003	Michael Setton	015290-756	3865

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EXAMINER	
POMPEY, RON EVERETT	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Office Action Summary	Application No. 10/622,652	Applicant(s) SETTON, MICHAEL	
	Examiner Ron E. Pompey	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

SUPPLEMENTAL DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 22-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester (US 5,200,352) or Jang (US 5,439,839) in view of Wu (5,880,508) and Moslehi (5,322,809).

a. Pfiester discloses the limitations of:

an interfacial layer (14, fig. 1A),on a silicon semiconductor substrate;

a gate electrode (16, fig. 1A) of an electrically conductive material, wherein the electrode is formed from a metal that is selected from the group consisting of doped polysilicon, TiN, W, Ta, Mo and multilayer thereof;

first (28, fig. 1D) and second (28, fig. 1D) lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

source and drain regions (32, fig. 1E) that are adjacent the gate electrode(col. 2, ln. 48 – col. 4, ln. 33);

a pair of first non-conductive spacers (20, fig. 1A), which comprise an oxide or nitride material, formed adjacent to the gate electrode and on the interfacial layer;

a pair of second non-conductive spacers (22, fig. 2) that is adjacent to the first spacers and the high dielectric, which also are formed over the lightly doped regions and on the interfacial layer(col. 5, lns. 30-41).

b. Jang discloses the limitations of:

an interfacial layer (22, fig. 3),on a silicon semiconductor substrate;

a gate electrode (20, fig. 4) of an electrically conductive material, wherein the electrode is formed from a metal that is selected from the group consisting of doped polysilicon, TiN, W, Ta, Mo and multilayer thereof;

first (80, fig. 5) and second (82, fig. 5) lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

source and drain regions (102 and 104, fig. 10) that are adjacent the gate electrode(col. 2, ln. 48 – col. 4, ln. 33);

a pair of first non-conductive spacers (21, fig. 7), which comprise an oxide or nitride material, formed adjacent to the gate electrode and on the interfacial layer;

a pair of second non-conductive spacers (85 and 87, fig. 8) that is adjacent to the first spacers and the high dielectric, which also are formed over the lightly doped regions and on the interfacial layer(col. 3, ln. 25 – col. 4, ln. 43).

3. Pfiester and Jang do not disclose the claimed limitation(s) of:

a high dielectric constant layer (2, fig. 5a), that comprises a material that is selected from the group consisting of Ta_2O_5 , Ta2 $(O_{1-x}\ N_x)_5$, a solid solution of $(Ta_2O_5)_r$ – $(TiO_2)_{1-r}$, a solid solution of $(Ta_2O_5)_s$ – $(Al_2O_3)_{1-s}$, a solid solution of $(Ta_2O_5)_t$ – $(ZrO_2)_{1-t}$, a solid solution of $(Ta_2O_5)_u$ – $(HfO_2)_{1-u}$, on the interfacial layer;

a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

a silicide layer on the source and drain regions;

an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface;

wherein the interfacial layer comprises silicon nitride or silicon oxynitride; and

a barrier layer between the gate electrode and the high dielectric constant layer. However,

a. Wu discloses the above claimed limitations regarding:

a high dielectric constant layer (8, fig. 1), that comprises a material of Ta_2O_5 , wherein the interfacial layer (6, fig. 1) comprises silicon nitride or silicon oxynitride;

a barrier layer (10, fig. 2) between the gate electrode and the high dielectric constant layer (column 2, line 63 – column 3, line 20); and

a gate electrode having a width of less than 0.3 micron (column 1, ln. 25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Pfiester or Jang with Wu, because the high dielectric constant layer provides for a gate insulator layer that reduces hot carrier effect; the barrier layer helps to provide better adhesion between the high dielectric constant layer and the gate; and the gate width of less than 0.3 micron take up less wafer real estate, which means more devices can be formed on one wafer.

b. Moslehi discloses the above claimed limitations regarding:

wherein the interlayer insulator is planar (46, fig. 3a) and silicide (41, fig. 2i) on the source and drain regions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Pfiester or Jang with Moslehi, because Moslehi the silicide on the source and drain provide for a lower resistivty for better electrical conduction for metal contact and the planar insulator keeps topography level so preceding layers can be uniform.

c. Neither Pfiester, Jang, Wu nor Moslehi disclose:

the various high dielectric compositions, consisting of $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less 1, a solid solution of $(Ta_2O_5)_u$-$(Hf0_2)_{l-u}$ wherein u ranges from about 0.9 to less than 1. However, applicant does not disclose that these materials will provide unique or different results, when used in a device, from the Ta_2O_5 material, listed in the group, disclosed by Wu. Therefore the other materials that are not shown by the prior arts of record are considered to be equivalent and obvious substitutes for the Ta_2O_5 disclosed in the prior art of record. Additionally no criticality has been placed on using one material over the other and therefore the substitution of one of the other claimed materials for the high dielectric layer does not provide patentable distinction from the material given in the prior arts of record.

Response to Arguments

4. Applicant's arguments, see page 14, line 5 through the bottom of page 15, filed April 12, 2005, with respect to the rejection(s) of claim(s) 22,38 and 39 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art references, because the new art discloses two sets of sidewall spacers in the configuration as claimed.

Allowable Subject Matter

5. Claims 41-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singly or in combination, fails to disclose the limitations of wherein the pair of second non-conductive spacers are formed on the interfacial layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on compressed.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ron Pompey
AU: 2812
July 27, 2005

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER